



### PRODUCT DESCRIPTION

The Infineon TriCore™ is an innovative, award-winning processor solution unifying the features of real-time microcontrollers, computational power of DSP and the price/performance benefits of a superscalar RISC. TriCore's modular system architecture facilitates the design of true system-on-chip solutions by enabling flexible integration with on-chip high-density memories, application specific peripherals, and customer logic.

TC1MP-S is the synthesizable implementation of the TriCore architecture and is now available as an XPack from IPextreme. The XPack is a complete configurable subsystem (available in either VHDL or Verilog) with an industry standard AMBA AHB interface, enabling simple integration into the wider platform, saving engineering effort and time to market.

### MCU FEATURES

- Fast context switch & low interrupt latency
- 16-bit and 32-bit instruction formats
- Powerful bit manipulation support

### DSP FEATURES

- Sustained throughput of two 16x16 MACs per clock
- SIMD packed arithmetic and zero overhead loops
- DSP addressing modes and saturated math

### PROCESSOR FEATURES

- 32-bit load-store Harvard architecture
- Superscalar execution
- 16 address and 16 data registers

### TRICORE BENEFITS

- Integrated MCU-DSP instructions in one core
- Fast & efficient processing of multiple tasks on one engine
- Low code size and inherent high-level language support
- One development toolset for both MCU and DSP tasks
- Higher flexibility and lower cost

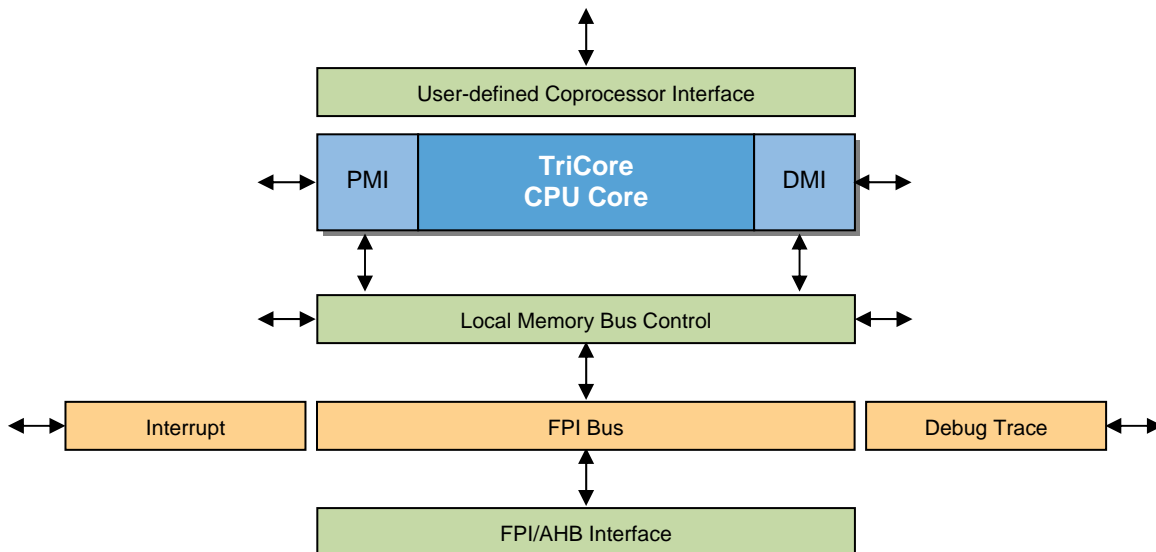
### TRICORE UNITS & INTERFACES

#### Superscalar Four-Stage Pipelined CPU

- 32-bit Load/Store Harvard Architecture
- 3 pipelines: Arithmetic, Load-Store, & Loop
- Single instruction Multiple Data capability

#### Control Features

- Single-bit addressing and manipulation
- Extract and insert data field instructions
- Fast context switching (from 4 cycles)
- 16 & 32-bit instructions, intermixable without boundary penalty



TriCore Block Diagram

## TRICORE UNITS & INTERFACES (CONTINUED)

### DSP Features

- Dual 16-bit Multiplier Accumulators
- Zero overhead loops
- Addressing: Circular, bit-reverse, register indirect with post & pre-increment
- Rounding, truncation, saturation, signed fraction support

### Memory Protection

- Native protection scheme
- Optional MMU Coprocessor Interface
- Up to 3 coprocessor available
- Floating Point coprocessor available

### Program Memory Interface (PMI)

- 64-bit interface for up to 64KB of configurable, tightly coupled cache/scratchpad memory

### Data Memory Interface (DMI)

- 128-bit interface for up to 64KB of configurable, tightly coupled cache/scratchpad memory

### Local Memory Bus (LMB)

- 64-bit data, 32-bit address
- Runs at CPU clock speed and supports 8, 16, 32 and 64-bit transfers
- Support for dual external interfaces Flexible Peripheral Interface (FPI) Bus
- 32-bit address and data de-multiplexed
- Single and multiple transfers: 8, 16 and 32-bit

### Interrupt Controller

- Programmable: Up to 255 Interrupt priorities/sources

### Debug Interface for Advanced Emulation

- Access to internal registers and memory through JTAG port
- Hardware, software and external breakpoints
- Support for trace functionality

## THE CUSTOMER EXPERIENCE

The IPextreme® engineering team has been creating quality IP for a decade, such as the first fully synthesizable ARM processor, the Infineon C166S, MPEG decoders, and Bluetooth. Our engineers understand integration challenges and so rework and package the design for maximum ease of use. They will typically limit parameters to those most important, simplify interfaces, bundle software, supply suites that verify connectivity, and generally transfer just the necessary knowledge from the original designers.

All the IP we ship is packaged in our patent pending XPack, which maximizes ease of use by letting the integration engineers configure complex IP through an intelligent user interface that outputs the configuration and constraints files for common tools

from Cadence, Mentor, and Synopsys. During the preparation and packaging of the IP our engineers learn enough about it to offer excellent support. IPextreme takes advantage of professional commercial IP delivery software systems and our engineers stick with the customer to ensure they successfully integrate IP purchased from us.

## XPACK TECHNOLOGY

XPack™ is an innovative technology from IPextreme that enables customers to quickly and easily integrate IP into their designs. This lightweight IP packaging technology is based on the familiar metaphor of a datasheet, which contains all the descriptions and diagrams one would expect from a datasheet; but in reality, it is the cockpit by which users interact with the IP. Customers change parameters or modify timing information by updating fields on the interactive datasheet; XPack then automatically generates code and scripts to reflect those changes.

XPack is the result of over a decade of experience delivering IP in the manner most readily usable by customers. IPextreme packages all its products with XPack technology.

## XPACK FEATURES

- Automatic configuration of source code based on user selectable options for both hardware and software parameters
- Generation of a instantiation template based on user configuration for the SoC design
- Generation of synthesis scripts and constraints for major EDA synthesis tools

## TRICORE XPACK CONTENTS

- RTL source code the baseband controller
- ANSI C source code for link manager software
- Integration test bench
- Self-checking integration tests
- Extensive user documentation

# IPextreme

### IPextreme, Inc.

307 Orchard City Drive  
Suite 202

Campbell, CA 95008  
800-289-6412 (toll-free)  
408-608-0421 (fax)

[www.ip-extreme.com](http://www.ip-extreme.com)

IPextreme is a registered trademark and XBlue, CoolBlue, and XPack are trademarks of IPextreme Inc. of Campbell, CA. All other trademarks are acknowledged.  
Copyright ©2006 IPextreme Inc. All rights reserved.