

With widespread adoption by semiconductor companies and support from leading software toolchain providers, Nexus 5001 is rapidly becoming the industry standard solution for embedded system software debugging. Nexus 5001 defines an IEEE global standard interface for real-time control and debug of multi-processor embedded systems. The benefit to developers is a common, low pin count, low cost interface that supports different microprocessor architectures and development tools.

Freescal Semiconductor, Inc. is a member of the Nexus 5001 Forum and provider of a wide range of Nexus 5001-enabled controllers. Freescal's Nexus 5001 IP for ARM cores is now available through IPextreme as a family of products that includes:

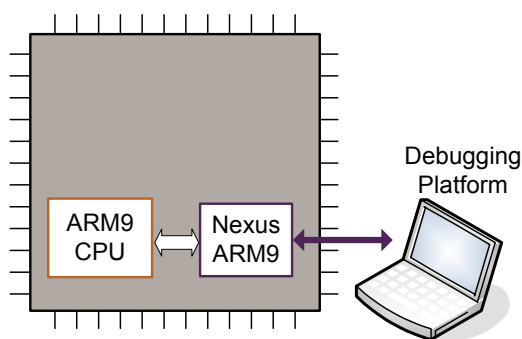
- ▶ Nexus ARM7: Client for ARM7
- ▶ Nexus ARM9: Client for ARM9
- ▶ Nexus AHB: Client for AMBA 2.0 AHB
- ▶ Nexus Port Controller: Enables dynamic sharing of one Nexus port between up to 8 Nexus clients

Availability of these Nexus components adds to the existing Nexus 5001 ecosystem. In addition, IPextreme can adapt Nexus clients for your processor or DSP.

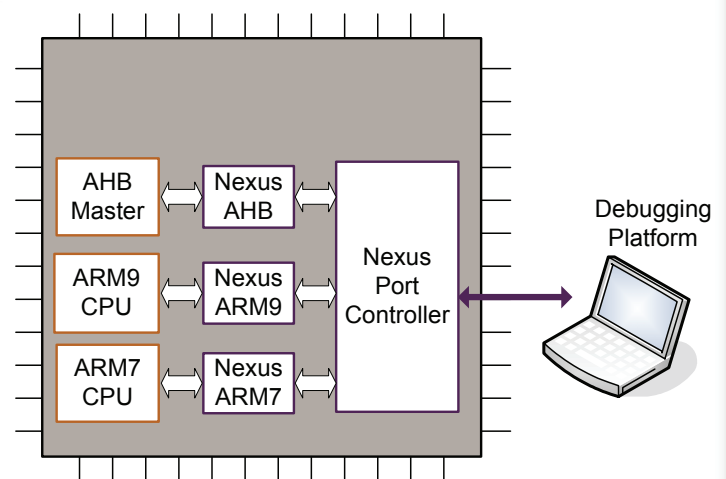


COMPARING TRADITIONAL DEBUG AND NEXUS 5001

Traditional Debug	Nexus 5001 Debug
Debug monitor: Requires code to be running in a functioning system; uses run-time resources; cannot debug ROM-based software	Nexus provides non-intrusive debug capability; provides visibility into CPU in any state; can debug ROM/boot code
In-circuit emulator: Expensive CPU-specific hardware; not portable to new projects; not suitable for integrated CPUs; too slow for modern systems	Standard debug interface supports evolution of both the processors and the debug tools; designed for access to embedded CPUs
Existing on-chip debug: Ad-hoc implementations with vendor-specific features and interfaces expensive to develop and port to new projects; often limited to one CPU per debug port	Nexus defines common feature set, register set, and uses standard JTAG port; IEEE standard and extensive ecosystem lowers cost; port controller enables multi-CPU debug from a single port



Single-Nexus Configuration

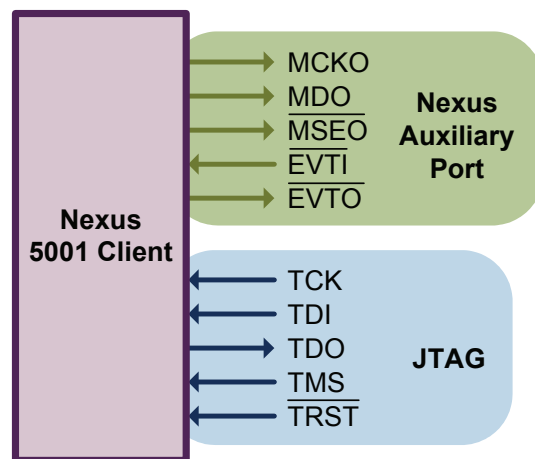


Multi-Nexus Configuration with Port Controller

NEXUS 5001

The Nexus 5001 Forum Standard for a Global Embedded Processor Debug Interface (IEEE-ISTO 5001 – 2003, available for download at www.nexus5001.org) defines 4 classes of feature sets. Each class is a superset of the features supported by the lower class(es).

When it is critical to minimize pin count, useful Class 1 functionality is delivered through an existing JTAG port. To support the external visibility required for the Class 2, 3, and 4 features, Nexus 5001 defines a Nexus Auxiliary Port to supplement JTAG with the fewest additional pins. The message data out (MDO) bit-width is scalable to support different bandwidths.

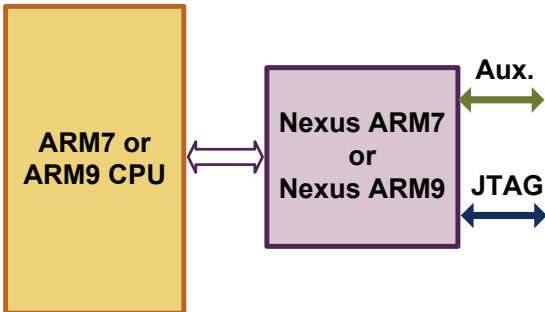


JTAG/Auxiliary Ports Implemented on Freescale Nexus 5001 IP from IPextreme

SUMMARY OF SUPPORTED NEXUS 5001 FEATURES BY CLASS				
Debug Feature	Class 1	Class 2	Class 3	Class 4
Read and write user registers in debug mode	√	√	√	√
Read and write user memory in debug mode	√	√	√	√
Enter debug mode from reset	√	√	√	√
Enter debug mode from user mode	√	√	√	√
Exit debug mode to user mode	√	√	√	√
Single-step instruction in user mode; re-enter debug mode	√	√	√	√
Stop execution on instruction/data breakpoint; enter debug mode	√	√	√	√
Set breakpoint or watchpoint	√	√	√	√
Device identification	√	√	√	√
Notify of watchpoint match	√	√	√	√
Monitor process ownership in real time (ownership trace)		√	√	√
Monitor program flow in real time (program trace)		√	√	√
Monitor data writes in real time (data trace)			√	√
Monitor data reads in real time (optional for Class 3 and 4)			√	√
Read and write memory in real time			√	√
Start ownership, program, or data trace on watchpoint				√
Control processor to avoid trace overruns				√

NEXUS ARM7 AND NEXUS ARM9

The Nexus ARM7 and Nexus ARM9 clients connect directly to an ARM7 or ARM9 processor, respectively, to support debugging through the standard Nexus 5001 interface.

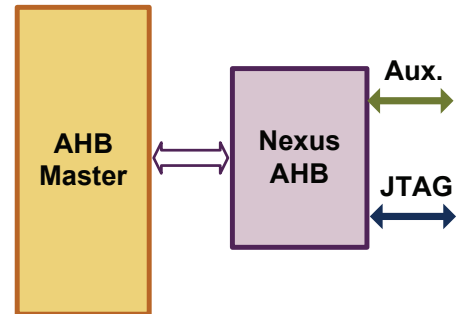


Debugging features of the Nexus ARM7 and Nexus ARM9 include:

- Compliant with Class 3 of IEEE-ISTO 5001 – 2003 (supports all Class 1/2/3 features)
- Also supports two Class 4 features:
 - Triggering of program/data trace on watchpoint
 - Processor overrun control
- Program Trace through Branch Trace Messaging
 - Branch/Predicate History Messaging in ARM mode
 - Branch History Messaging Direct/Indirect Branch Messaging in Thumb mode
- Data Trace through Data Read/Write Messaging
- Ownership Trace through Ownership Trace Messaging
- Run-time access to the memory map through JTAG port
- Watchpoint Messaging through auxiliary pins
- Breakpoint on instruction address
- Bit-widths of auxiliary pins MSEO and MDO are configurable
- Registers for Program Trace, Ownership Trace, Watchpoint Trigger, and Read/Write Access
- Programmable processor stall function to mitigate message queue overrun risk
- All features controllable and configurable through JTAG port

NEXUS AHB FOR REAL-TIME AHB TRACE

The Nexus AHB module monitors AHB transactions from an AHB master such as a DMA controller, providing real-time trace information to your debugging tool.

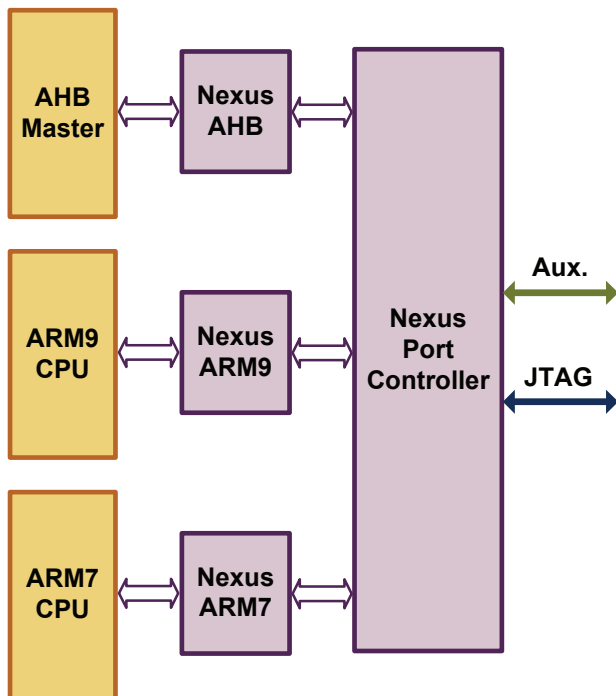


Features of the Nexus AHB include:

- Data Trace through Data Read/Write Messaging
- Two internally generated address/data watchpoints
- Four externally (SoC) generated watchpoints
- Watchpoint Messaging through auxiliary pins (internal and external watchpoints)
- Watchpoint Trigger enable of Data Trace Messaging
- Auxiliary interface for higher data throughput
- Registers for Data Trace, Watchpoint generation, and Watchpoint Trigger
- All features controllable and configurable through JTAG port or memory-mapped interface
- Timestamp capability on all message types
- Control for SoC-level debug (through EVTO)

NEXUS PORT CONTROLLER

The Nexus Port Controller is not specific to the ARM/AHB architecture. It is a CPU-neutral switching module that enables up to 8 Nexus clients to dynamically share a single interface to the debugging platform.



Features of the Nexus Port Controller include:

- Arbiter for the Nexus Auxiliary Port
- Uses internal or external (SoC) TAP controller
- Nexus Device ID Register and Messaging
- Controls Auxiliary Port configuration (MDO port width and MSEO configuration)
- Generates MCKO controls
- Controls sharing of EVTO output
- Controls the device-wide debug request from Nexus clients
- Generates asynchronous reset signal for Nexus blocks based on Test-Logic-Reset state, disable input signal, and power-on reset status
- Generates a timestamp value for use by Nexus clients. Triggering mechanism is available to control timestamp counter start/stop.

NEXUS 5001 IP INTEGRATION OPTIONS

- Single Nexus 5001 connection for single CPU
- With Port Controller for dynamic access to multiple Nexus clients through a single shared port

CONFIGURABILITY

Hardware parameters for:

- Implementation of selected registers
- Size of message queues
- JTAG instruction ID for Nexus access

Control pins to set:

- MSEO width (1 or 2 bits)
- MDO width (8 or 16 bits)
- Single- or multi-Nexus connection
- Use of internal or external JTAG TAP controller

APPLICATIONS

Suitable for any embedded system requiring real-time debug capability, including:

- Automotive applications, where Nexus is a de facto requirement
- Industrial control systems
- Communications
- Computer peripherals
- Consumer electronics

DELIVERABLES

Each of the Nexus 5001 IP components is delivered as a separate design package that includes:

- Synthesizable RTL source code (Verilog)
- Documentation
- Integration testbench
- IPextreme XPack packaging technology for design configuration, simulation, and synthesis with support for common EDA tools

DEBUG TOOL SUPPORT

Several leading toolchain providers are members of the Nexus 5001 Forum and currently provide tools that support the Nexus standard for various processor architectures.



WIND RIVER

Contact your development tool provider for information regarding Nexus 5001 support.

For the current list of Nexus 5001 Forum members, including development tool providers, go to www.nexus5001.org.

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