INTERCONNECT MIXES IP FOR MULTIMEDIA

The relentless march of Moore's Law over the last few decades has enabled the implementation of amazingly sophisticated functionality at consumer price points such as HDTVs, DVD recorders and PDA phones

Unfortunately, manufacturable gate counts have grown far faster than IC designers' productivity over the past decade. With so much pressure to launch high-end consumer products before prices erode, standards change, trends or popularity phases end or counterfeit competition surfaces, every aspect of the design flow requires analysis to see how time-to-silicon can be shortened.

property). Modern SoC designs often contain multiple processor cores of varying types, which raise a myriad of issues that must be addressed during the entire design process from specification to implementation.

A systematic development approach (figure 1) can lay a solid foundation for design productivity, but cannot always cope with the exponential complexity arising from

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Recent history shows that the most successful high-end consumer products relied on the rapid acquisition, integration, optimisation, and verification of key functionality as semiconductor IP (intellectual

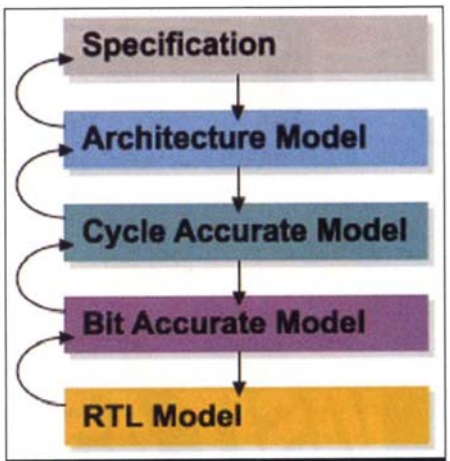

Figure 1: The systematic approach

the integration of many cores into one system chip. One solution is to decouple function from dataflow. Functions are typically implemented in the form of IP blocks that are traditionally connected over on-chip buses, tightly coupling the dataflow to the function. New forms of on-chip communications use a network fabric, instead of on-chip buses, to connect the IP blocks together and tune the system performance and latency.

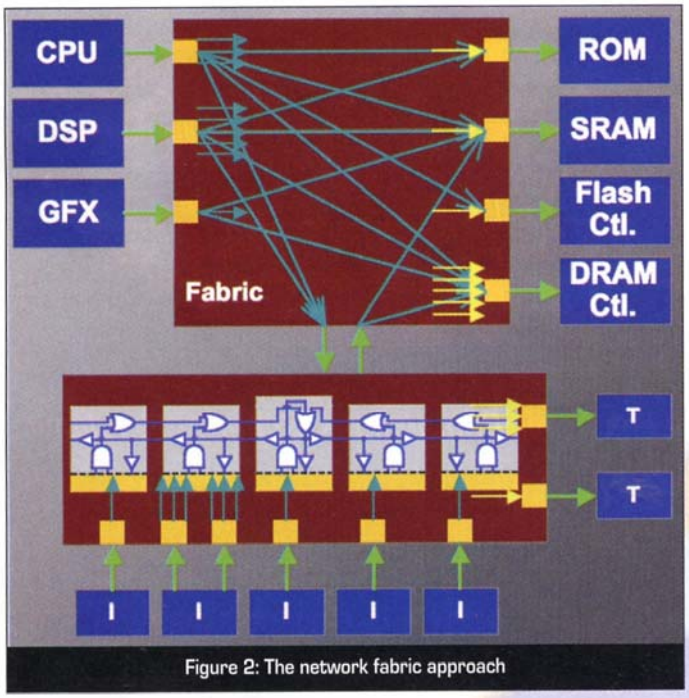

Figure 2: The network fabric approach

A network fabric, as shown in figure 2, can be used connect IP blocks to form a system. Crossbar switches connect IP with high-throughput or low-latency requirements, while slower peripherals are connected through a shared link. System performance requirements can be easily decomposed into a set of connectivity requirements and the fabric automatically generated with the correct characteristics to optimise performance, latency, and power consumption.

There are many benefits to the approach of decoupling function from dataflow at both the design level and in the final silicon. They include power management, variable security features (e.g. for digital rights management), improved reuse of IP blocks from one generation SoC to the next, and increased flexibility for optimisation.

Figure 3 illustrates how IP blocks can be partitioned along the lines of function and communication boundaries. The IP function is attached to the communications layer over a standard OCP (Open Core Protocol) interface. The communication layer sits between the OCP layer and the network fabric. All the intelligence and flexibility for communicating with the fabric is isolated in the communication layer. Different communication layers can support multiple

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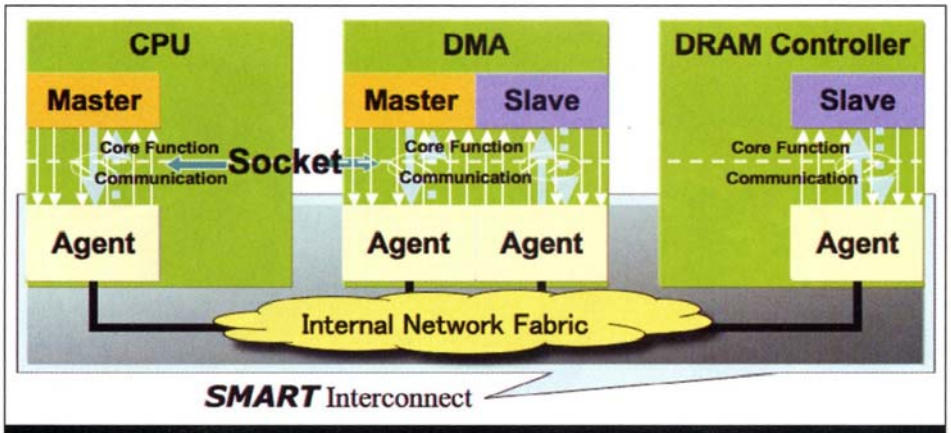

Figure 3: Decoupling function from communication

on-chip protocols (e.g. AMBA, CoreConnect) that can attach the IP block without modification due to the standard nature of OCP.

Decoupling the functional aspects of the IP block from the communication aspects represents only one dimension of the IP design task. The designer must anticipate other design issues beyond dataflow requirements.

Planning IP

IP is often configurable allowing its use in a variety of applications. This includes not only configuration of the RTL but also of the associated firmware, drivers, diverse data flow requirements, and tests. Developers need to develop a plan that envisions hardware/software partitioning to show what configurations will be locked in hardware and what will be configured in software that can be changed at the board level and over the course of the chip's life.

Proprietary interfaces should be avoided wherever possible to maximise reusability. Standard interfaces (e.g. AMBA, CoreConnect) provide means for plug-and-play for simple systems whereas OCP can provide the ability to plug into these simple systems as well as take advantage of sophisticated, multi-threaded, non-blocking data flow interconnect capabilities of network fabrics.

Partitioning can minimise fab-specific sections. Ideally these are avoided altogether, or at least isolated from the fully reusable sections of the IP. To keep chips using IP more generally applicable, process specific portions such as memory interfaces and clock gating logic should be brought to top-level ports of the core.

One good practice is to provide integration tests that follow the IP configuration. It is much easier for the integrator if the test bench automatically tests only for the configured functions and just gives a simple pass/fail result. This requires integration tests that are based on the configuration settings.

The complexity of common electronic devices like mobile phones is not apparent to most people. Figure 4 shows the complexity of a high-end mobile phone processor that contains a large number of different IP blocks that must all communicate efficiently.

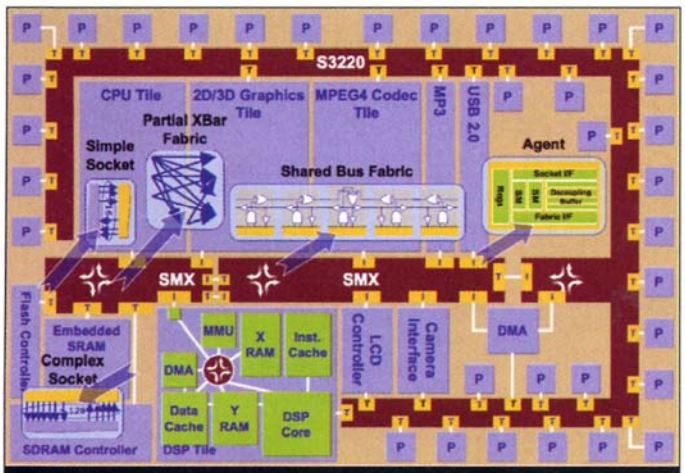

Figure 4: A mobile phone processor

Each block is a standalone function and is connected to other blocks over an intelligent network fabric. This structure can provide architects with a great freedom to quickly develop optimised variations on the same basic design. For example, high-end designs may employ an MPEG4 decoder for video, while low-end designs can be derived by subtracting the video capability and re-optimising inter-block communication to reduce power.

A key advantage of modular design is that, using standard interfaces and network fabrics, it enables teams to work independently on different aspects of the design. Many efforts may proceed in parallel instead of sequentially, greatly reducing time to functional, optimised silicon. Even if different aspects of the design flow require tweaking and iteration, the process is greatly shortened and simplified.

A modular approach also allows new IP blocks to be added or subtracted to create special versions of the IP for different markets and allow the designs to be reused for successive generations of projects.

The semiconductor industry is facing increased competitive pressure to provide more complex and differentiated solutions in time for ever-shorter market windows. The key to survival is to adopt a design process that best uses the available technology to achieve advantage over competitors. Intelligently developed and packaged IP blocks connected through sophisticated socket-based network fabric enable SOC engineers to assemble great new consumer electronic systems, faster and more economically than ever before.

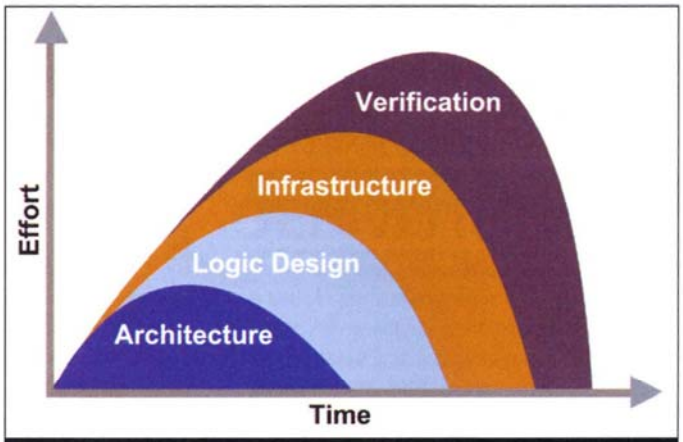

Figure 5: The advantages of model design

JEFF HAIGHT is director, technical marketing, Sonics Inc; Warren Savage is president and CEO, IPextreme Inc